In the Claims

Cancel claim 13, and amend claims 1, 3, 4, 7, 9, 11, 12, 17, 20 and 22 as follows:

1. (currently amended) A metrology target mask for determining proper lithographic exposure dose ~~and/or~~and focus in a pattern formed in a layer on a semiconductor substrate by lithographic processing comprising:

a mask substrate;

a first, dose and focus sensitive mask portion on the mask substrate having a first array of elements comprising a plurality of spaced, substantially parallel elements having essentially the same length and width, ends of the individual elements being aligned to form first and second opposing array edges, the pitch of said first array of elements being selected such that, when lithographically printed in a layer on a semiconductor substrate, first array of elements are resolvable, with the lengths of and spaces between said elements being sensitive to both dose and focus of an energy beam ~~when lithographically printed in a layer on a semiconductor substrate~~; and

a second, dose sensitive mask portion on the mask substrate having a second array of elements comprising a central element having a length and a width, and a plurality of spaced, substantially parallel outer elements, each having a length and a width, the widths of the outer elements being less than the width of the central element, edges of the outer elements on each side of and farthest from the central element forming opposing array edges, the pitch of said outer elements being selected such that, when lithographically printed in a layer on a semiconductor substrate, the

outer elements are not resolvable ~~after lithographic printing in a layer on a semiconductor substrate~~ and width of the ~~resulting printed~~ second ~~target~~ portion ~~width~~ is sensitive to dose but not focus of the energy beam,

wherein, after projecting an energy beam through the mask and lithographically printing the mask portions in a layer on a semiconductor substrate and determining the widths of the first and second target portions in the layer by measuring distance between opposing array edges in each of the first and second portions, dose ~~and/or~~and focus of the energy beam during lithographic processing of said layer ~~may~~ can be determined.

2. (original) The mask of claim 1 wherein the edges of the array in the first mask portion are substantially parallel to edges of the array in the second mask portion, and the elements in the first mask portion are substantially perpendicular to the elements in the second mask portion.

3. (currently amended) The mask of claim 1 wherein pitch between elements of the arrays in the second mask ~~sensitive~~ portion is less than the resolution limit of the energy beam ~~in the imaging system~~ used to expose the mask in the lithographic processing.

4. (currently amended) The mask of claim 1 wherein the second, dose sensitive mask portion includes a plurality of outer elements on each side of said central element, the widths of the outer elements decreasing with distance from the central element.

5. (original) The mask of claim 1 wherein the elements of the first and second mask portions comprises opaque elements on a substantially transparent mask substrate.

6. (original) The mask of claim 1 wherein the elements of the first and second mask portions comprises substantially transparent elements on an opaque mask substrate.

7. (currently amended) A metrology target mask for determining proper lithographic exposure dose ~~and/or~~and focus in a pattern formed in a layer on a semiconductor substrate by lithographic processing comprising:

a mask substrate;

a first, dose and focus sensitive mask portion on the mask substrate having a first array of elements comprising a plurality of spaced, substantially parallel elements having essentially the same length and width, ends of the individual elements being aligned to form first and second opposing array edges, the pitch of said first array of elements being selected such that, when lithographically printed in a layer on a semiconductor substrate, first array of elements are resolvable, with the lengths of and spaces between said elements being sensitive to both dose and focus of an energy beam ~~when lithographically printed in a layer on a semiconductor substrate~~; and

a second, dose sensitive mask portion on the mask substrate having a second array of elements comprising a central element having a length and a width, and a plurality of spaced, substantially parallel outer elements having a length and a width, the

outer elements being substantially perpendicular to the central element, ends of the outer elements farthest from the central element being aligned to form first and second opposing array edges, the pitch of said outer elements being selected such that, when lithographically printed in a layer on a semiconductor substrate, the outer elements are not resolvable ~~after lithographic printing in a layer on a semiconductor substrate~~ and width of the ~~resulting printed~~ second ~~target~~ portion ~~width~~ is sensitive to dose but not focus of the energy beam,

wherein, after projecting an energy beam through the mask and lithographically printing the mask portions in a layer on a semiconductor substrate and determining the widths of the first and second target portions in the layer by measuring distance between opposing array edges in each of the first and second portions, dose ~~and/or~~and focus of the energy beam during lithographic processing of said layer can ~~may~~ be determined.

8. (original) The mask of claim 7 wherein the edges of the array in the first mask portion are substantially parallel to edges of the array in the second mask portion, and the elements in the first mask portion are substantially perpendicular to the outer elements in the second mask portion.

9. (currently amended) The mask of claim 7 wherein pitch between outer elements of the arrays in the second dose sensitive mask portion is less than the resolution limit of the energy beam ~~in the imaging system~~ used to expose the mask in the lithographic processing.

10. (original) The mask of claim 8 wherein the outer elements on the second, dose sensitive mask portion are tapered.

11. (currently amended) A metrology target for determining proper lithographic exposure dose ~~and/or~~and focus in a pattern formed in a layer on a semiconductor substrate by lithographic processing comprising:

a substrate;

a first, dose and focus sensitive target portion in a lithographically formed layer on the substrate having a first array of elements comprising a plurality of spaced, substantially parallel elements having essentially the same length and width, ends of the individual elements being aligned to form first and second opposing array edges, the pitch of said first array of elements being selected such that, when lithographically printed in a layer on a semiconductor substrate, first array of elements are resolvable, with the lengths of and spaces between said elements being sensitive to both dose and focus of an energy beam ~~when lithographically printed in a layer on a semiconductor substrate~~; and

a second, dose sensitive target portion in the lithographically formed layer on the substrate having a single element having a length and a width, edges along the length of the single element forming opposing array edges, the width of the single element being sensitive to dose but not focus of the energy beam when lithographically printed in a layer on a semiconductor substrate,

wherein, after determining the widths of the first and second target portions in the layer by measuring distance between opposing array edges in each of the first and second portions, dose ~~and/or~~and focus of the energy beam used during lithographic processing of said layer can ~~may~~ be determined.

12. (currently amended) The target of claim 11 wherein the edges of the array in the first target portion are substantially parallel to edges of the single element array in the second target portion, and the elements in the first target portion are substantially perpendicular to the element~~s~~ in the second target portion.

13. (cancelled)

14. (original) The target of claim 11 wherein the substrate is electrically non-conductive, the elements in each of the first and second target portions are electrically conductive, and the elements in the first array are electrically connected, and wherein, upon applying a current across each of the arrays and measuring the voltage, the suitability of the layer ~~may~~ can be determined by the resistance of each of the arrays.

15. (original) The target of claim 14 wherein each target portion has a first end and a second end, the target portions being electrically connected at the second ends, and including electrically conductive pads at the first end of each of the target portions and the connected second ends of the target portions such that current may be applied

between the pads on the target portion first ends and voltage may be measured between the first and second ends of each of the targets.

16. (original) The target of claim 15 wherein the elements in the first target portion are electrically connected by an electrically conductive central element, and wherein the individual elements of the first target portion extend in a perpendicular direction from each side of the first target portion central element.

17. (currently amended) A method of determining proper lithographic exposure dose ~~and/or~~and focus in a pattern formed in a layer on a semiconductor substrate by lithographic processing, the method comprising:

providing a semiconductor substrate;

providing the metrology target mask of claim 1;

projecting an energy beam through the mask onto the semiconductor substrate;

lithographically forming a target in a layer on the semiconductor substrate having first and second target portions corresponding to the first and second mask portions, respectively;

determining the widths of the first and second target portions in the layer by measuring distance between opposing array edges in each of the first and second portions; and

using the measured widths of the first and second target portions in the layer to determine dose ~~and/or~~and focus of the energy beam used during lithographic processing of said layer.

18. (original) The method of claim 17 wherein the elements of the second, dose sensitive mask portion are not resolved by the energy beam in forming the corresponding second target portion, and wherein the second target portion comprises a single element formed in the layer on the semiconductor substrate having a length and a width, with edges along the length of the single element forming opposing array edges.

19. (original) The method of claim 18 wherein the edges of the array in the first target portion are substantially parallel to edges of the array in the second target portion, and the elements in the first target portion are substantially perpendicular to the element in the second target portion.

20. (currently amended) A method of determining proper lithographic exposure dose ~~and/or~~and focus in a pattern formed in a layer on a semiconductor substrate by lithographic processing, the method comprising:

providing a semiconductor substrate;

providing the metrology target mask of claim 7;

projecting an energy beam through the mask onto the semiconductor substrate;

lithographically forming a target in a layer on the semiconductor substrate having first and second target portions corresponding to the first and second mask portions, respectively;

determining the widths of the first and second target portions in the layer by measuring distance between opposing array edges in each of the first and second portions; and

using the measured widths of the first and second target portions in the layer to determine dose ~~and/or~~and focus of the energy beam used during lithographic processing of said layer.

21. (original) The method of claim 20 wherein the elements of the second, dose sensitive mask portion are not resolved by the energy beam in forming the corresponding second target portion, and wherein the second target portion comprises a single element formed in the layer on the semiconductor substrate having a length and a width, with edges along the length of the single element forming opposing array edges.

22. (currently amended) A method of electrically testing image shortening of a pattern formed on a substrate by lithographic or etch processing comprising:

providing the ~~electrically conductive~~ target of claim ~~17~~ 14;

applying a current across the first and second target portions;

measuring the voltage drop and determining the resistance across each of the first and second target portions; and

determining the suitability of the layer by the resistance of the first and second target portions.

23. (original) The method of claim 22 wherein there is determined the suitability of energy beam dose or focus on a lithographically formed layer.